UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/585,512	07/10/2006	Tsutomu Sakakibara	071971-0660	4161

53080 7590 08/17/2009

MCDERMOTT WILL & EMERY LLP
600 13TH STREET, NW
WASHINGTON, DC 20005-3096

EXAMINER	
SNYDER, ADAM J	
ART UNIT	PAPER NUMBER
2629	

MAIL DATE	DELIVERY MODE
08/17/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/585,512	SAKAKIBARA ET AL.	
	Examiner	Art Unit	
	Adam J. Snyder	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 15* is/are pending in the application.

4a) Of the above claim(s) *5-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 July 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. Figures 29 and 30 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1, 2, and 15** are rejected under 35 U.S.C. 102(b) as being anticipated by Matsushima et al (US 6,437,766 B1).

Claim 1, Matsushima (Fig. 1 and 2) discloses a drive device (Fig. 1) comprising:

a first generation section (11-1 through 11-257; wherein elements produce signals P1-P256) for sequentially turning k first signals (P1-P256; wherein k is 256) from a non-output state to an output state (wherein figure 2 shows P1-P156 going from a non-output state to output state) according to a first clock (Fig. 2; wherein CLK is used to generate signals P1-P256 sequentially), where k is a natural number (wherein 256 is a natural number);

a second generation section (Col. 9, Line 6-8; wherein produces signals G1-G4) for sequentially turning m second signals (G1-G4; wherein m is 4) from the non-output state to the output state (wherein figure 2 shows G1-G4 going from a non-output state to output state) according to a second clock (Fig. 2; wherein T is used to generate signals G1-G4 sequentially; Col. 9, Line 66-Col. 10, Line 4), where m is a natural number (wherein 4 is a natural number); and

(k×m) (Col. 9, Lines 3-5; GP1-GP1024) output circuits divided into k groups (wherein figure 1 shows 256 groups),

wherein m output circuits (12-1 through 12-1056) belong to each of the k groups (wherein figure 1 shows four AND gates are connected to each of the 256 groups),

the k first signals (P1-P156) correspond to the k groups (wherein figure 1 shows P1-P256 connected to 256 groups),

the m second signals (G1-G4) correspond to the m output circuits (12-1 through 12-1056) belonging to each of the k groups (wherein figure 1 shows G1-G4 connected to 256 groups), and

each of the (k×m) (Col. 9, Lines 3-5; GP1-GP1024) output circuits:

outputs its corresponding second signal when the second signal is turned to the output state if the first signal corresponding to the group to which the output circuit belongs is in the output state (Fig. 2; wherein figure 2 shows when both G1 and P1 is high out GP1 is high), and

does not output its corresponding second signal even when the second signal is in the output state if the first signal corresponding to the group to which the output circuit belongs is in the non-output state (Fig. 2; wherein figure 2 shows when G1 is high and P2 is low then GP5 is not output).

Claim 15, Matsushima (Fig. 1 and 2) discloses a drive method (Fig. 2) for sequentially outputting drive signals (GP1-GP1024) from (k×m) output terminals divided into k groups (wherein figure 1 shows 256 groups), where k and m are natural numbers (wherein 256 and 4 are natural numbers), m output terminals (wherein 4 output terminals GP1-GP1024 belong with each group) belonging to each of the k groups (wherein figure 1 shows 256 groups), the method comprising:

sequentially turning k first signals (Fig. 2; P1-P256; wherein k is 256) corresponding to the k groups (wherein figure 1 shows 256 groups) from a non-output state to an output state (wherein figure 2 shows P1-P156 going from a non-output state to output state) according to a first clock (Fig. 2; wherein CLK is used to generate signals P1-P256 sequentially);

sequentially turning m second signals (Fig. 2; G1-G4; wherein m is 4) corresponding to the m output terminals (12-1 through 12-1056) belonging to each of the k groups (wherein figure 1 shows four AND gates are connected to each of the 256 groups) from the non-output state to the output state (wherein figure 2 shows G1-G4 going from a non-output state to output state) according to a second clock (Fig. 2; wherein T is used to generate signals G1-G4 sequentially; Col. 9, Line 66-Col. 10, Line 4); and

in each of the (k×m) output terminals (Col. 9, Lines 3-5; GP1-GP1024), outputting the second signal corresponding to the output terminal from the output terminal as the drive signal when the second signal is turned to the output state if the first signal corresponding to the group to which the output terminal belongs is in the output state (Fig. 2; wherein figure 2 shows when both G1 and P1 is high out GP1 is high); and

in each of the (k×m) output terminals (Col. 9, Lines 3-5; GP1-GP1024), not outputting the second signal corresponding to the output terminal from the output terminal as the drive signal even when the second signal is in the output state if the first signal corresponding to the group to which the output terminal belongs is in the non-

output state (Fig. 2; wherein figure 2 shows when G1 is high and P2 is low then GP5 is not output).

Claim 2, Matsushima (Fig. 1 and 2) discloses wherein the second generation section sequentially turns the m second signals (Col. 9, Line 6-8; wherein produces signals G1-G4) from the non-output state to the output state (wherein figure 2 shows G1-G4 going from a non-output state to output state) according to the second clock (Fig. 2; wherein T is used to generate signals G1-G4 sequentially; Col. 9, Line 66-Col. 10, Line 4) during the time when any one of the k first signals is in the output state (wherein figure 2 shows producing signals G1-G4 during any one of P1-P256 signals).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claim 3** is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushima et al (US 6,437,766 B1) in view of Murakami et al (JP 05-313129 A).

Claim 3, Matsushima discloses the drive device of Claim 1.

Matsushima does not expressly disclose wherein each of the (k×m) output circuits includes:

an output terminal;

a first input terminal for receiving the second signal corresponding to the output circuit;

a first switch connected between the output terminal and the first input terminal for switching ON/OFF according to the state of the first signal corresponding to the output circuit;

a second input terminal for receiving a predetermined voltage corresponding to the non-output state of the second signal, and

a second switch connected between the output terminal and the second input terminal for switching ON/OFF according to the state of the first signal corresponding to the output circuit.

Murakami (Fig. 8, 1, 2, 5, and 9) discloses wherein each of the (k×m) output circuits (Fig. 9a and 9b) includes:

an output terminal (OUT);

a first input terminal (A) for receiving the second signal (V1) corresponding to the output circuit (Fig. 2);

a first switch (Te or Tg) connected between the output terminal (OUT) and the first input terminal (A) for switching ON/OFF (Paragraph [0010]; wherein Sc controls out state input terminals) according to the state of the first signal (Sc) corresponding to the output circuit (Fig. 2);

a second input terminal (B) for receiving a predetermined voltage (i.e. ground) corresponding to the non-output state of the second signal (wherein second terminal is selected and while not outputting the second signal), and

a second switch (Tf or Th) connected between the output terminal (OUT) and the second input terminal (B) for switching ON/OFF (Paragraph [0010]; wherein Sc controls out state input terminals) according to the state of the first signal (Sc) corresponding to the output circuit (Fig. 2).

At the time of the invention was made, it would have been obvious to a person of ordinary skill in the art to modify Matsushima's gate control device by applying an output control circuit, as taught by Murakami, so to use a gate control device with an output control circuit for providing a high definition display, without increasing substantially the number of lessening the number of scan driver IC and attaining low-pricing, or scan driver IC (Paragraph [0006]).

8. **Claim 4**, is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushima et al (US 6,437,766 B1) in view of Morita (US 7,079,122 B2).

Claim 4, Matsushima discloses the drive device of Claim 1.

Matsushima does not expressly disclose wherein the first generation section includes k first flipflops connected in series, and

the second generation section includes m second flipflops connected in series.

Morita (Fig. 14) discloses wherein the first generation section includes k first flipflops connected in series (FFB0-FFBQ; wherein each block contains one control flip-flop), and

the second generation section includes m second flipflops connected in series (FF1-FF8; wherein each block contains eight row control flip-flips).

At the time of the invention was made, it would have been obvious to a person of ordinary skill in the art to modify Matsushima's gate control device by using flip-flops, as taught by Morita, so to use a gate control device with flip-flops for driving the plurality of scan lines sequentially in a designated block at the time of the partial display mode produces a high image quality and a low power consumption compatibility (Col. 3, Lines 37-42; Col. 2, Lines 30-31).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adam J. Snyder whose telephone number is (571) 270-3460. The examiner can normally be reached on M-F (8:30am-5pm) EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/AJS/
Examiner, Art Unit 2629
08/12/2009

/Chanh Nguyen/
Supervisory Patent Examiner, Art Unit 2629